Electron beam lithography for GaAs and GaN HEMT

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Outline

- HEMTs
- EBL technique
- GaAs T- gates
- GaN T-gates
- Conclusions

High-electron-mobility transistors

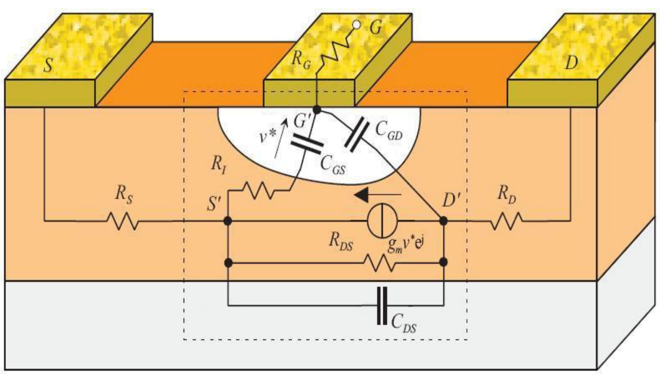
HEMTs

GaAs, GaN

high frequency

application in wireless communications, defense industry, satellites and RADARs

T/R modules based on high power amplifiers (HPA) and low noise amplifiers (LNA).



2DEG density is modulated by V_G

HEMTs are normally “ON” for $V_G = 0$

Pinch–off for $V_G = V_{PO} < 0$

Why GaAs and GaN?

1)

	Si	GaAs	GaN
E_g (eV)	1.1	1.42	3.39
μ_n (cm^2/Vs)	1350	8500	2000
ν_e (x10^7 cm/s)	1.0	1.0	1.5
E_{bd} (MV/cm)	0.3	0.4	3.3
Θ (W/cmK)	1.5	0.43	1.3

GaAs: high mobility

GaN: high breakdown, thermal conductivity, electron velocity

2) 2DEG GaAs/AlGaAs and GaN/AlGaN heterostructures: improvement of device performance ⇨

HIGH FREQUENCY

HIGH POWER DEVICES

GaN more expensive than GaAs

At fixed power GaN amplifier are smaller: costs reduction

Why Electron Beam Lithography?

HEMT

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

$$C_{GS} \, \alpha \, L_G$$

$$f_{MAX} = \frac{f_T}{2\sqrt{r_1 + f_T \tau_3}}$$

Cutoff frequency f_T is in inversely proportional to gate length L_G

Scaling down the gate length is required to improve the device performances and increase the frequency

EBL

- high resolution on large area
- versatile tool for R&D
- no mask set are required

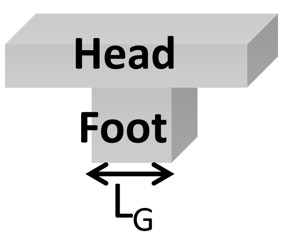
Why T-gate?

Gate fabrication is critical to achieve high HEMT performances

Goal: reduced gate resistance and parasitic capacitance
to reach high RF gain and control short channel effects

Fabrication of **T-gate** (field-plate) electrodes

1) Single EBL exposure: Trilayer resists, different sensitivities, metallization, lift-off
2) Double EBL exposure: «Foot» exposure, etch and thin metallization, lift-off
«Head» exposure, metallization, lift-off



R_g
C_{gs}

Mix & Match: EBL and stepper lithography
- optimization of alignment process and markes
- direct writing on 2”, 3”, 4” substrates

• optimization of EBL on insulating and conductive substrates

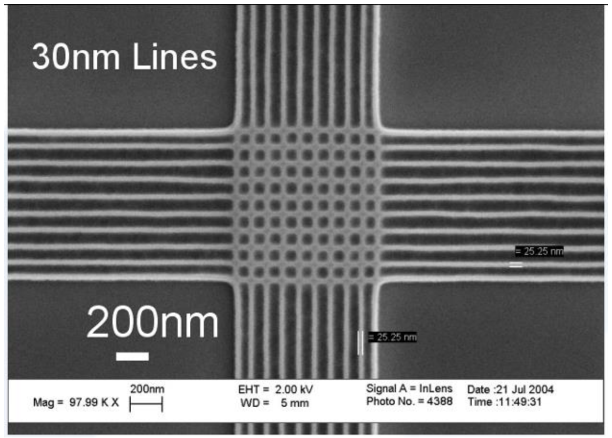
Electron Beam Lithography

Vistec EBPG 5HR

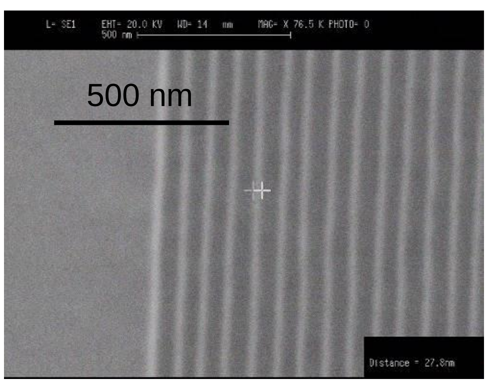
- field emission gun (FEG)
- 100kV
- beam diameter: 8 nm
- overlay accuracy <50nm
- 10 MHz max frequency
- block size 560 μm
- laser interferometer (λ /120~5nm) + pull-in system
- laser height sensor
- wafer size up to 4”
- mask writing
- markers alignment

Electron Beam Lithography

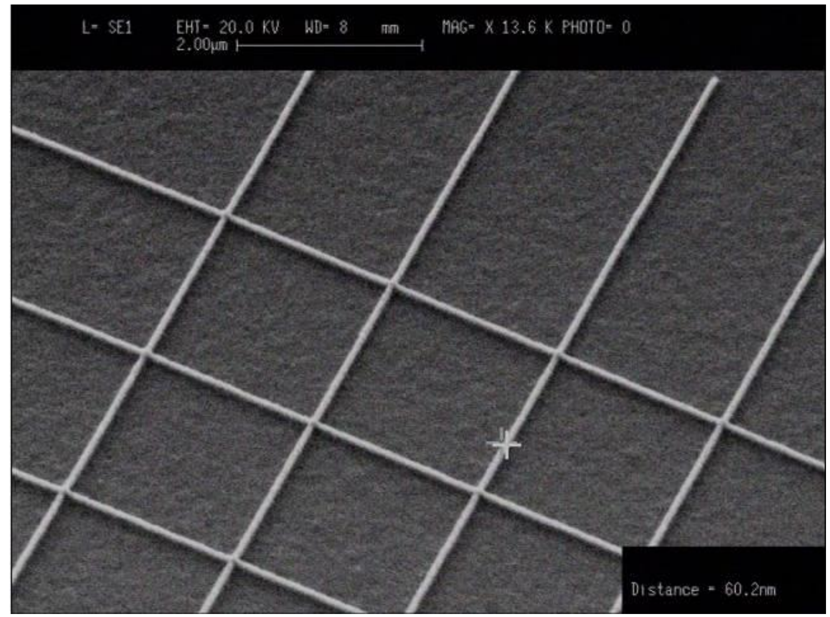
HSQ resist 30nm



TiAu 30nm



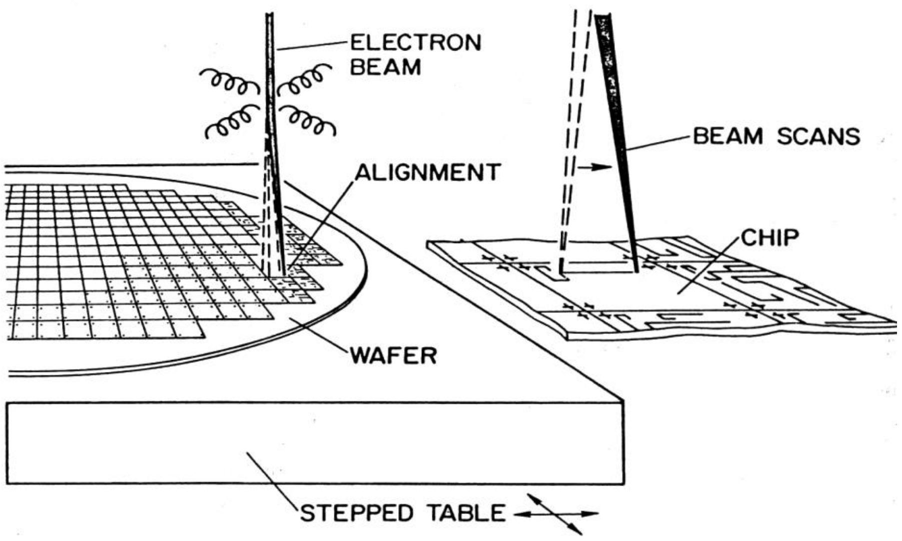
Si wires 60nm



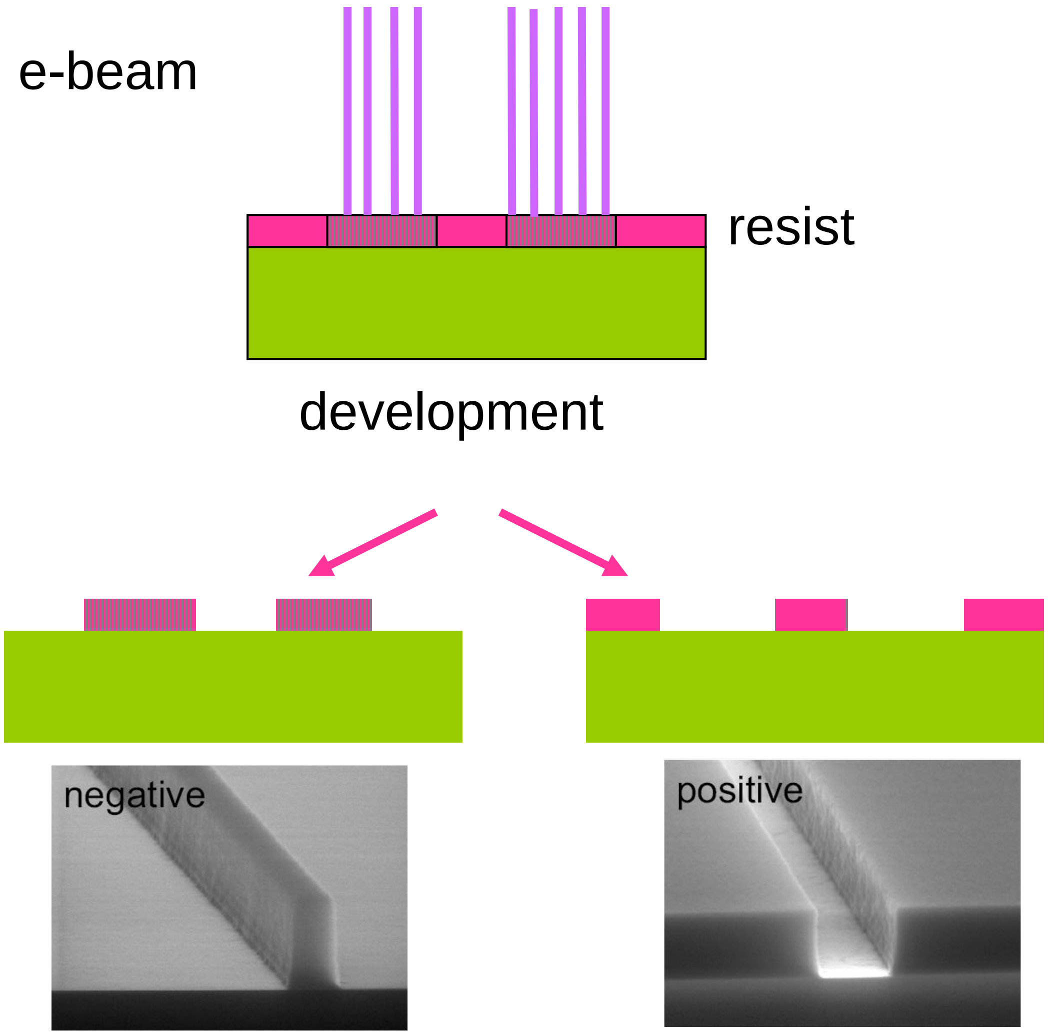
Electron Beam Lithography

- The e-beam is deflected by magnetic lenses to expose the resist
- The maximum area of beam deflection is called **field**
- A field is exposed without stage movement

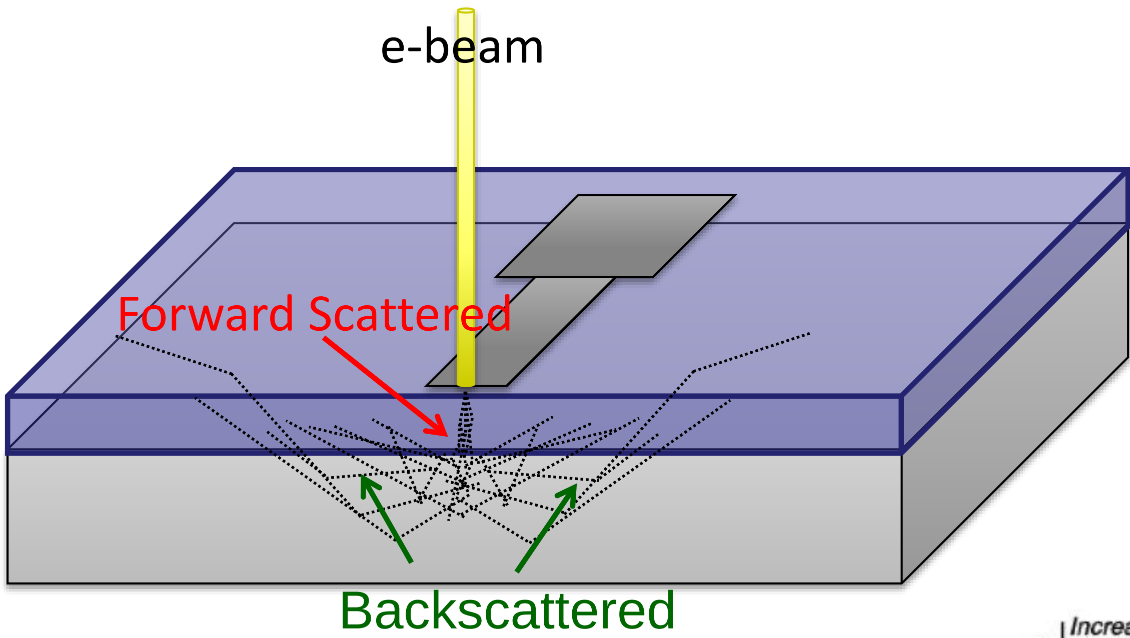
- Larger areas are divided in **fields** and the sample is moved to expose each field
- Correction systems avoid **sticthing** errors between fields

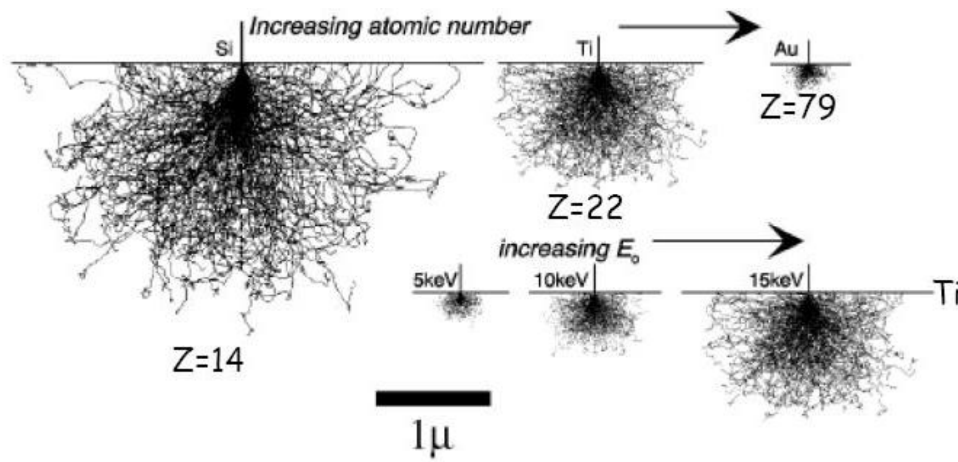


Electron Beam Lithography

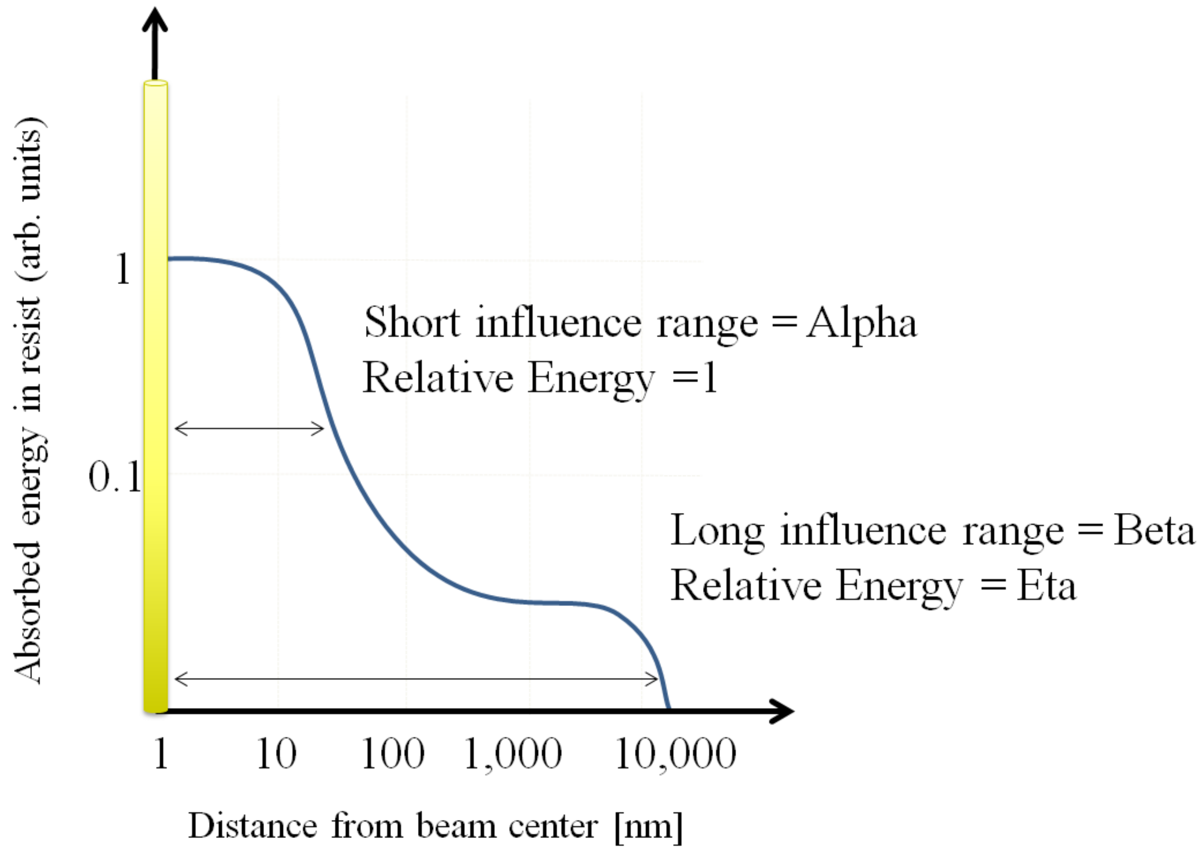


Proximity effect



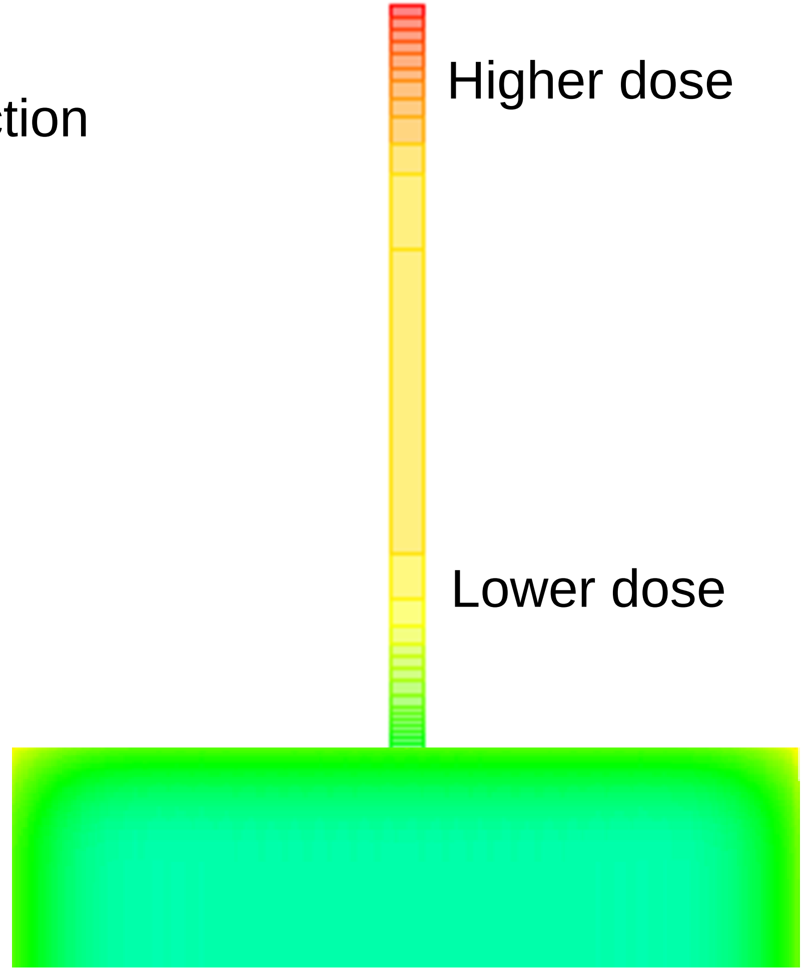


Energy distribution



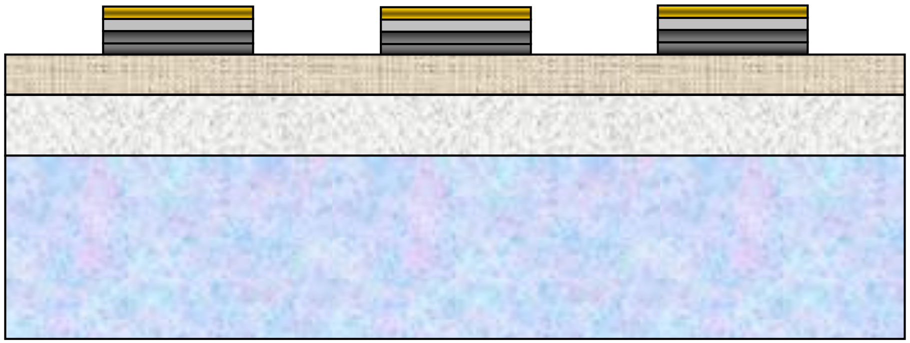
Proximity effect correction

Software for dose correction

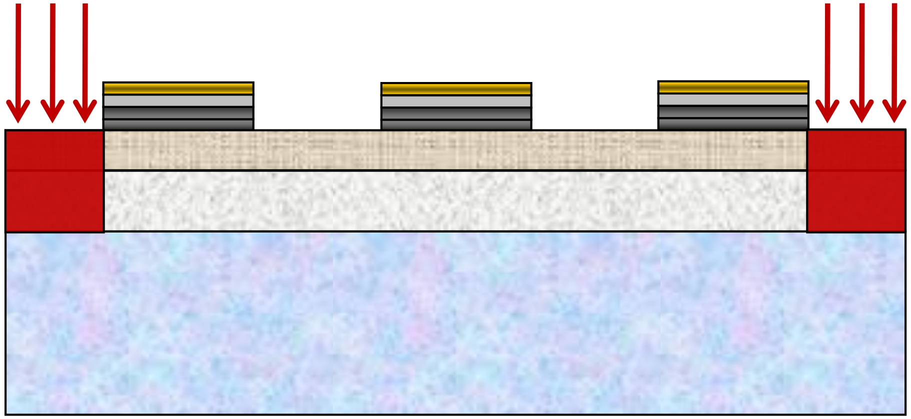


Devices fabrication

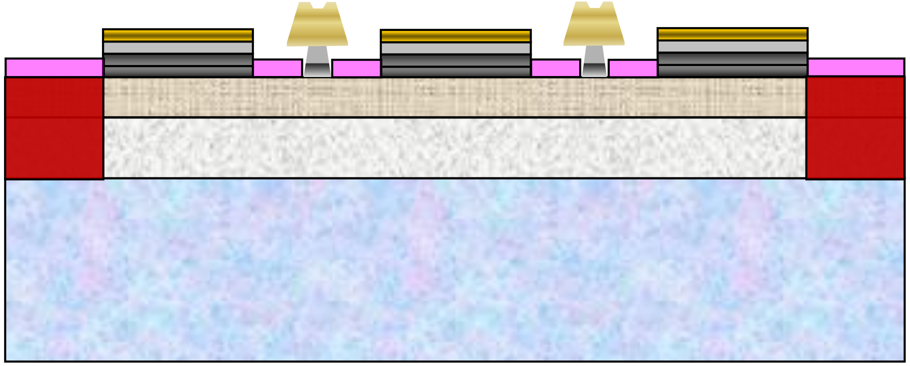
➢ Ohmic contact definition



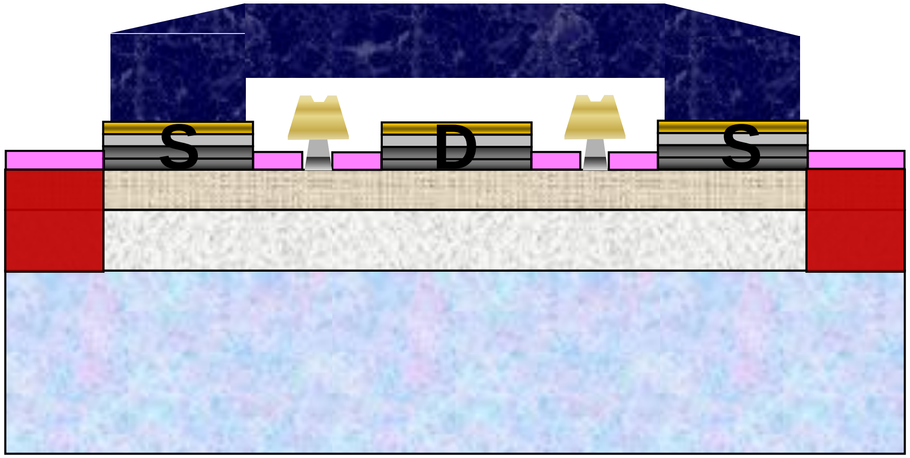
➢ Isolation



➢ Gate fabrication

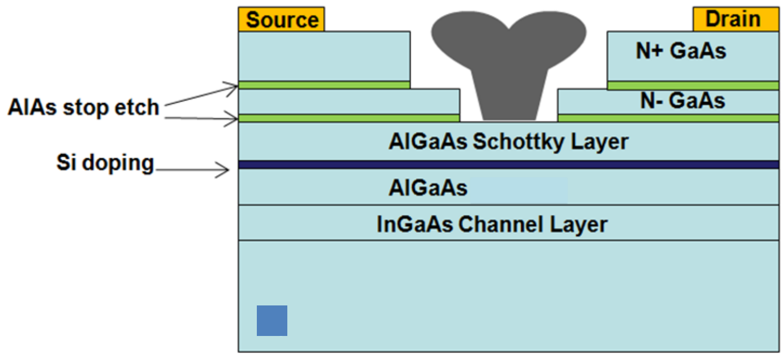


➢ Overlay and tick metal connection

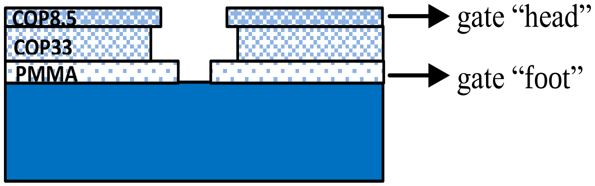


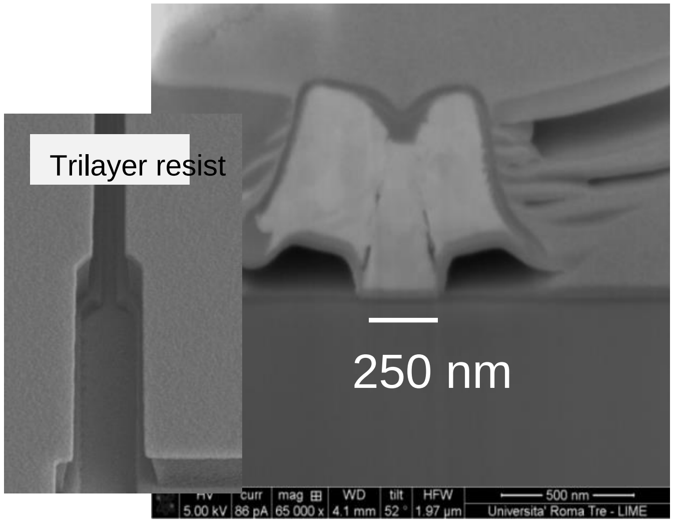
GaAs gate

➢ T-Gate shape (C_{gs} , R_g)



- ✓ Double Recessed Gate technology
- ✓ Low resistance contact





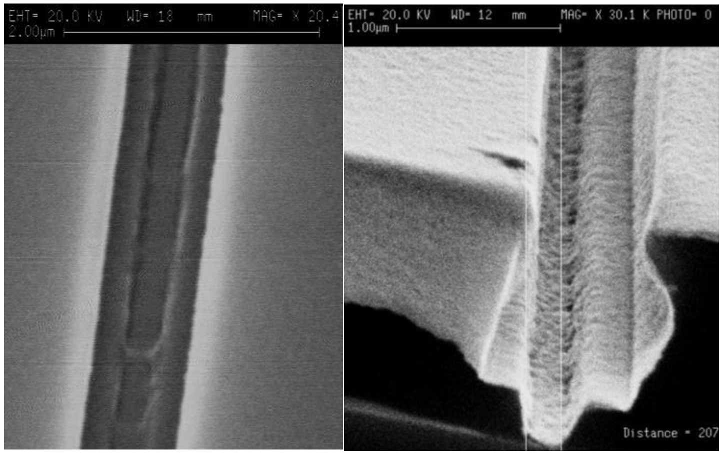
T-gate

Single e-beam writing

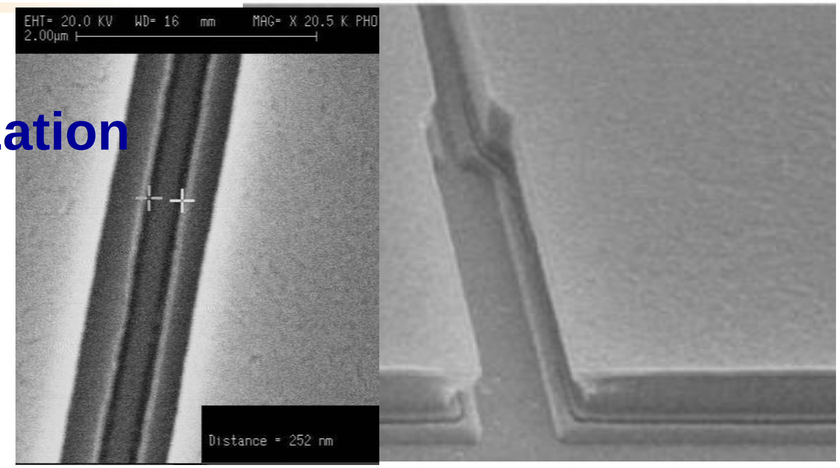
- Trilayer PMMA/COP33/COP8
- EBL
- Development and metallization

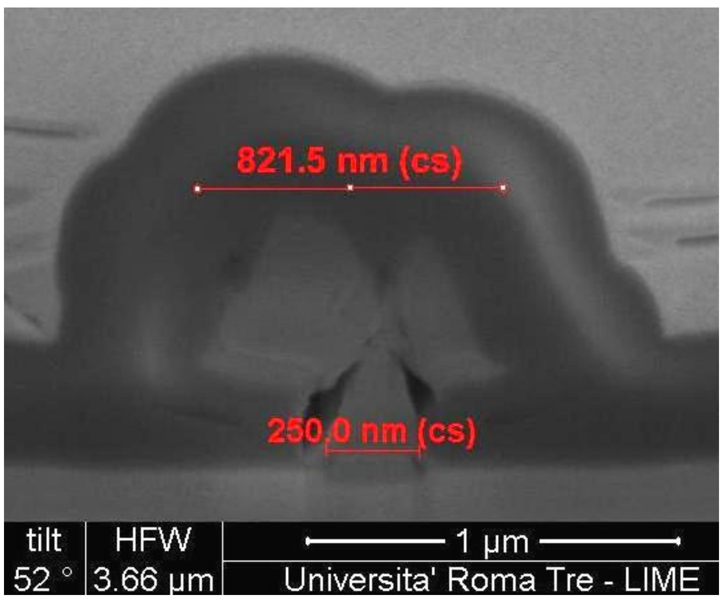
✓High Yield/Reproducibility
✓High Gain for High Frequency Operation
✓High Power Performance

Dose optimization for GaAs substrates

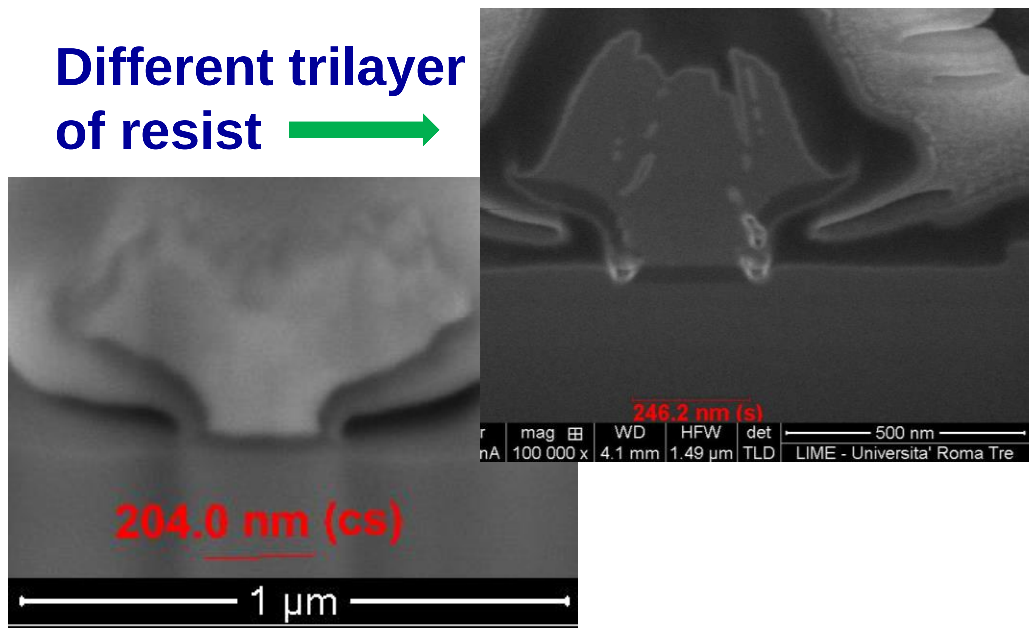


Dose optimization →

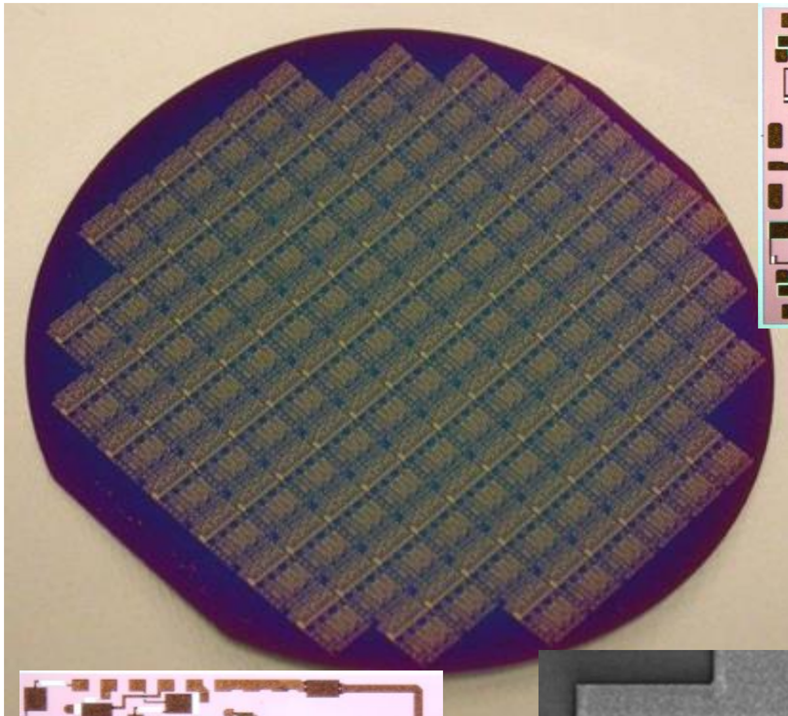


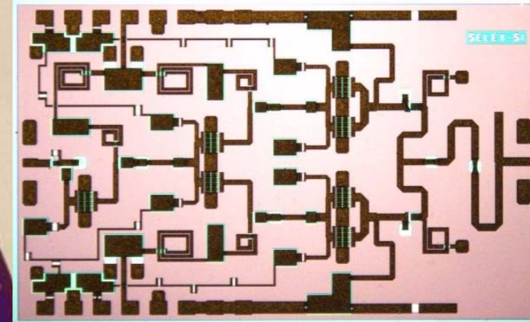


Different trilayer of resist →

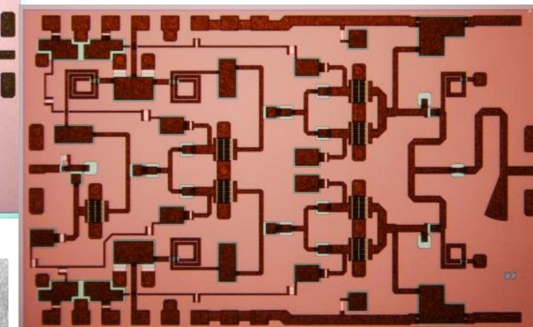


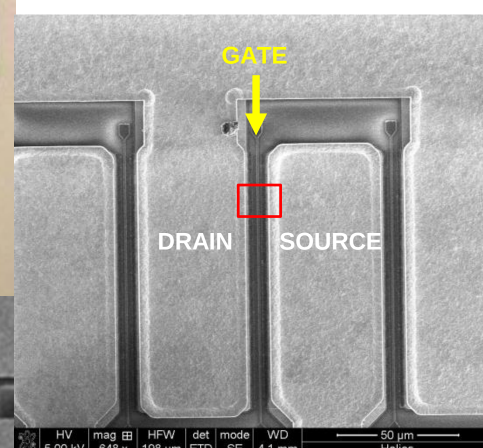
GaAs devices

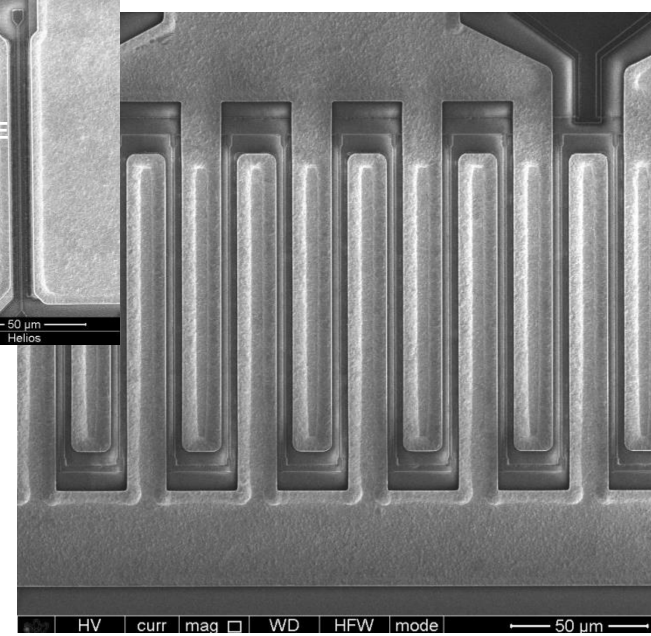


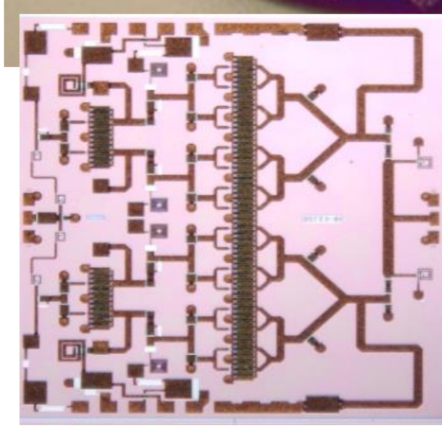


Large band

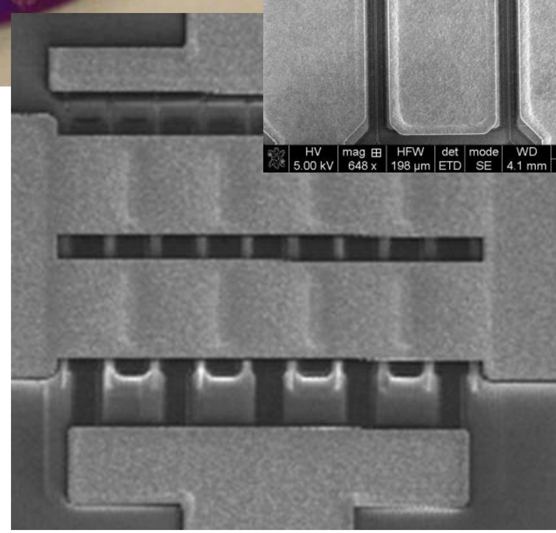








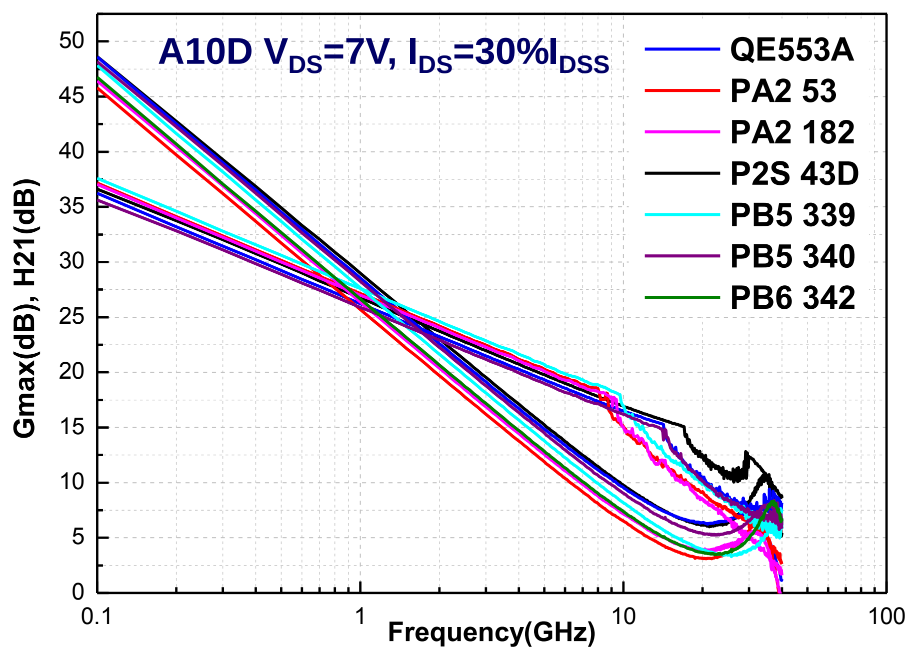
X-Band



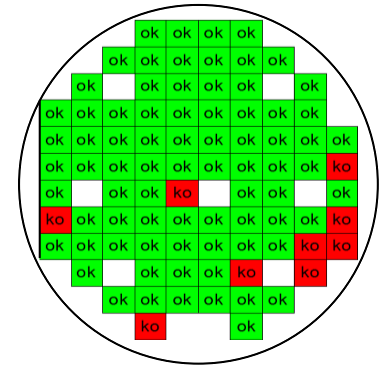
HPA's performances

HPA prototypes for different application band
Lg=250nm

Application	Output Power (dBm)	Gain (dB)	PAE (%)	Chip size (mm x mm)	Yield	Total Gate Periphery (mm)
6-18GHz HPA	34±1	>17	24±4	4.8 x 2.8	85%	7.0
4.5-18GHz HPA	33±1	>16	25 ± 5	5.2 x 2.9	85%	7.0
X-Band HPA	40.8±0.5	>18	35±2	3.8 x 4.2	>75%	26.4

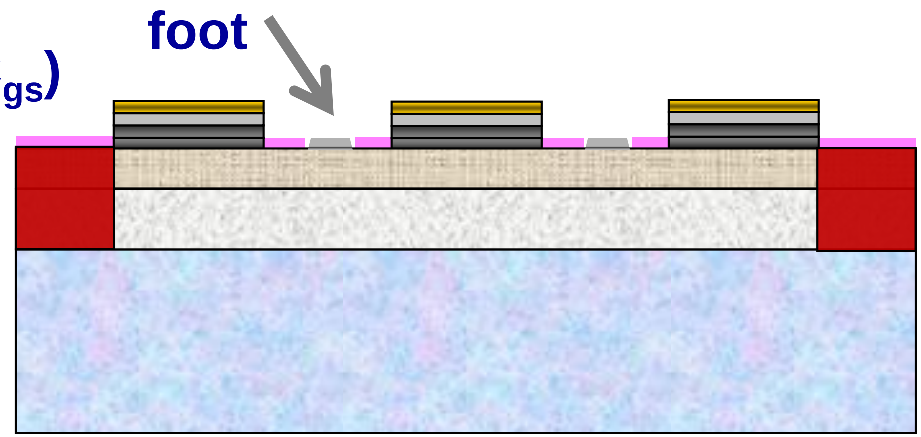


High on-wafer yield even for large total gate periphery

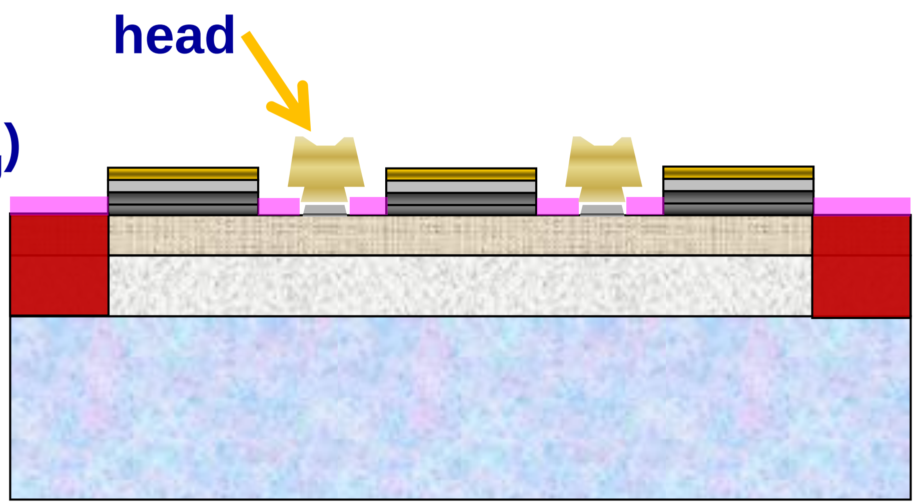


GaN gate

- 1° EBL Gate-foot definition (C_{gs})
  - ✓ Bilayer PMMA/COP8/Cr
  - ✓ Plasma etch
  - ✓ Thin metallic bilayer (Ni/Pt)
  - ✓ Annealing

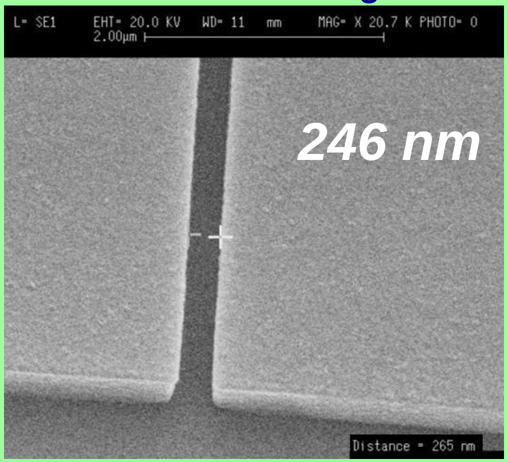


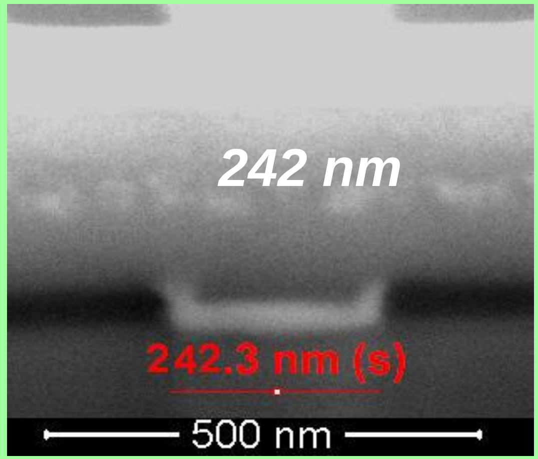
- 2° EBL Gate-head shaping (R_g)
  - ✓ T-gate
    PMMA/COOP/COP8/Cr
  - ✓ Alignment foot/head
  - ✓ Thick metal (Ni/Au)

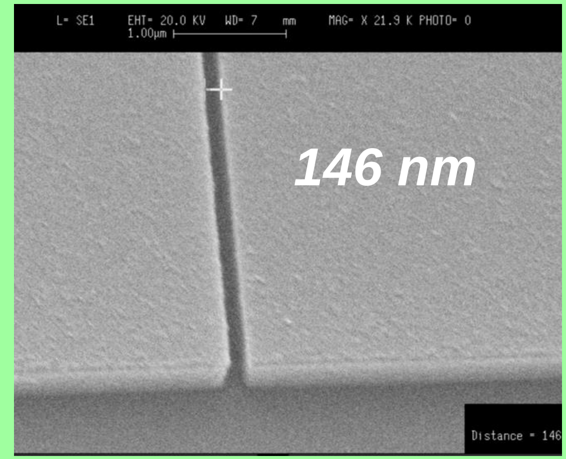


Dose optimization for GaN substrates

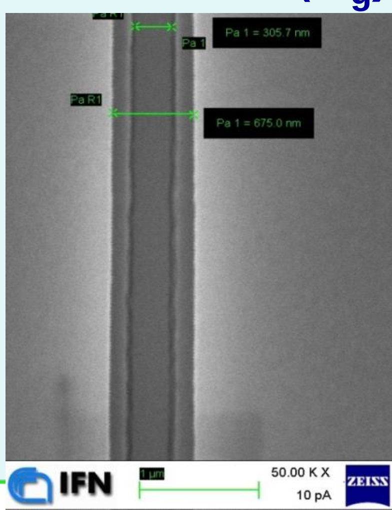
Gate-“foot” (C_{gs})

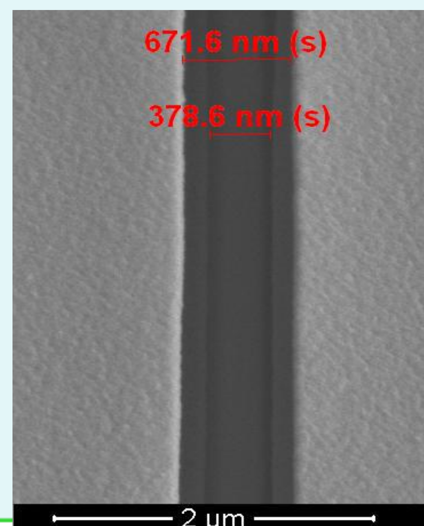


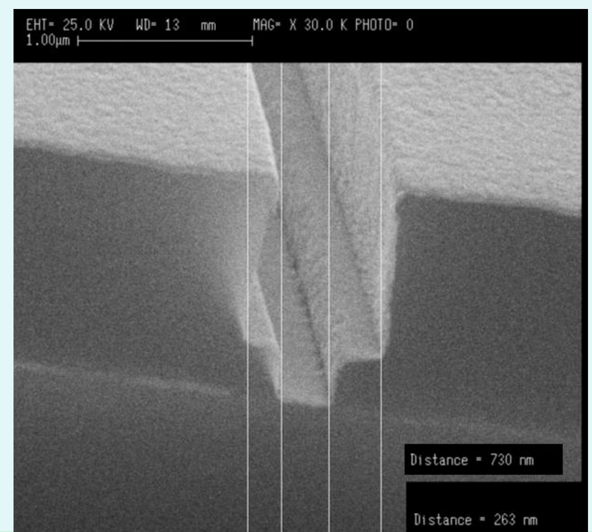




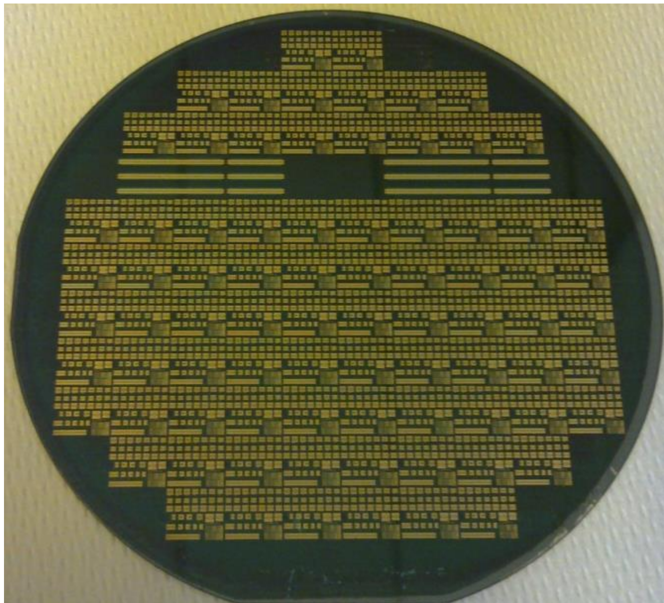
Gate-“head”(R_g)



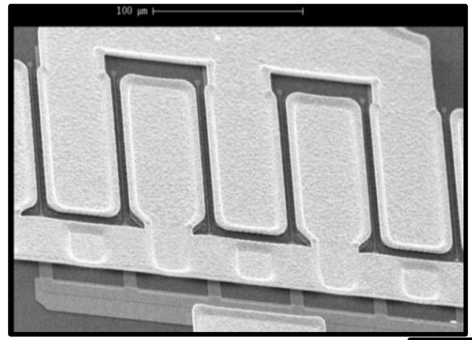


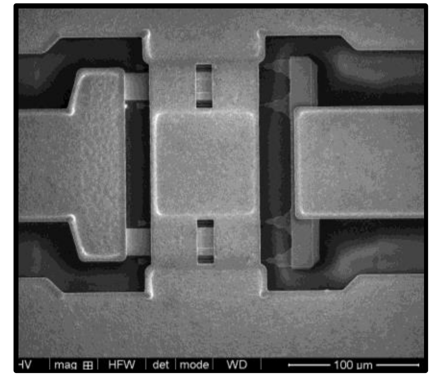


GaN devices

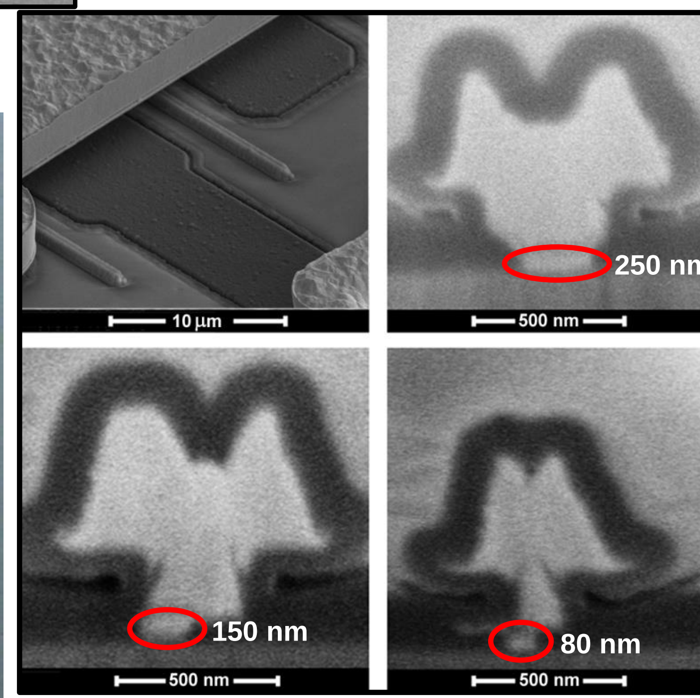


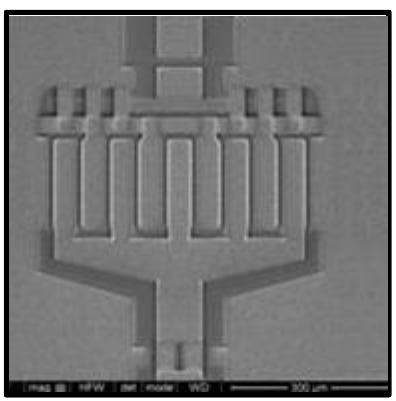
6x75 µm



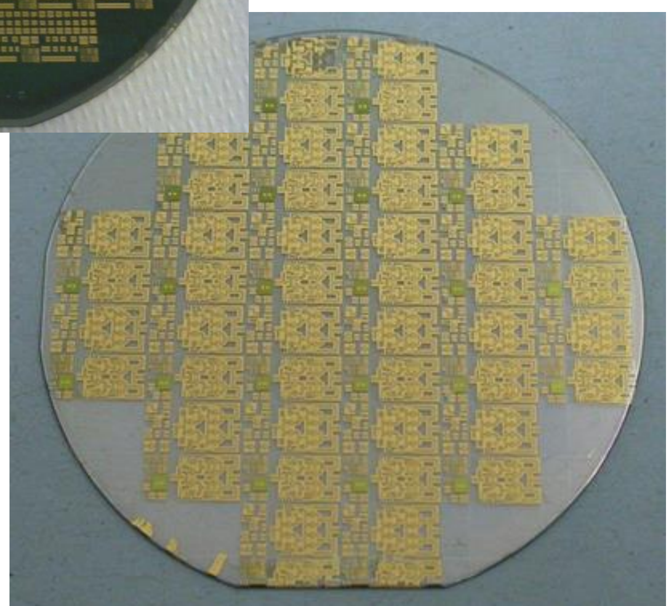


2x50 µm



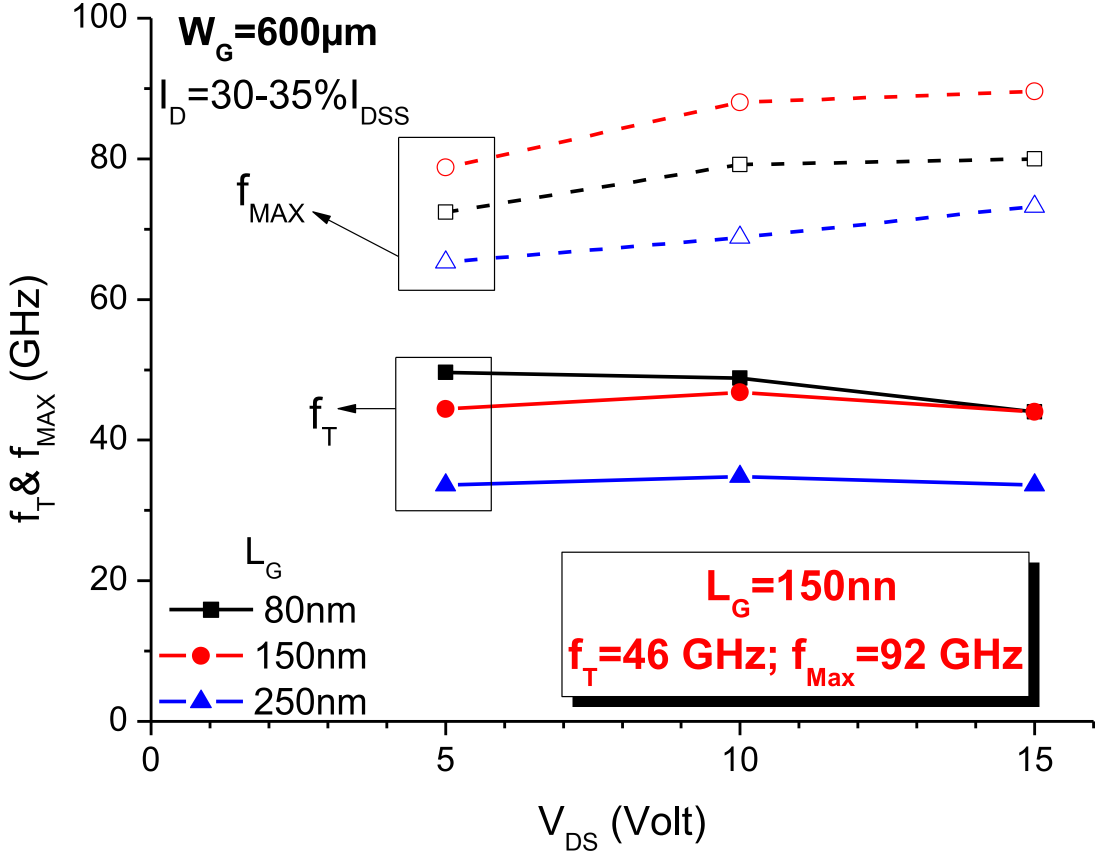


10x100 µm



RF characterization

LG=250-150-80 nm devices with 10x75µm, 8x75µm and 4x75µm gate periphery



8x75µm

By decreasing the Lg, the f_T is increased while the best result for f_{MAX} is with L_g=150nm

Conclusions

- **Fabrication and optimization of T-gates, footprint down to 80nm, on GaAs and GaN HEMT**

- **Technology transfer research-industry**

- **EBL based field plate technology is now used in standard Leonardo Foundry production of GaN and GaAs HEMT Lg=0.25um**

Thanks for the attention!

Raith 5150 EBL